REMARKS

In the Office Action, the Examiner rejects claims 1-4, 6, 7, 16, 18 and 19 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication 2003/0151077 to Matthew et al. ("Matthew") in view of U.S. Patent No. 5,663,586 to Lin ("Lin").

By this Amendment, Applicants have canceled claims 2 and 19 without prejudice or disclaimer and amended claims 1 and 16 to include certain features from now-canceled claims 2 and 19. Claims 1, 3, 4, 6, 7, 16, and 18 remain pending.

The rejections of claims 2 and 19 under 35 U.S.C. § 103(a) are obviated by virtue of their cancellation.

Regarding pending claims 1, 3, 4, 6, 7, 16, and 18, the Examiner essentially maintained the previous rejections of these claims based on Matthew and Lin. Applicants respectfully disagree with the Examiner's rationale for maintaining this rejection and request, for the following reasons, that the Examiner reconsider and withdraw the rejections.

Claim 1, as amended, recites, among other things, a first sidewall spacer having a substantially triangular shaped cross-section and a second sidewall spacer having a substantially triangular shaped cross-section, and "wherein the first and second sidewall spacers cause a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers to reduce micromasking effects during etching of the gate." The Examiner appears to contend that Mathew discloses these features. (Office Action, page 2). Applicants respectfully disagree and submit that Mathew does not disclose or suggest this feature. More specifically, Matthew does not even discuss the desirability of causing a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers, and certainly does not disclose doing so to reduce micromasking effects during etching of the gate.

Arguments similar to those made above were made in the previous Amendment After Final of November 22, 2005. In response, the Examiner contends that this feature of claim 1 is disclosed by Mathew and that the recitations of claim 1 relating to "reducing micromasking effects" "does not structurally define over Mathew's spacers 62' and 64'." (Office Action, page 6). Additionally, in the Continuation Sheet to the Advisory Action of December 8, 2005, the Examiner appears to contend that the Manocha patent (U.S. Patent No. 4,807,013) would in some way lead one of skill in the art to interpret Mathew to disclose sidewall spacers that cause a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers, as recited in claim 1. Applicants respectfully disagree with the Examiner's analysis.

Mathew completely fails to in any way disclose or suggest reducing micromasking, the desirability of reducing micromasking effects, or the formation of first and second sidewall spacers to cause a topology of a gate to smoothly transition over a fin and first and second sidewall spacers to reduce micromasking effects during etching of the gate. Mathew merely discloses a double-gate FinFET type MOSFET. FinFETs are discussed in Applicants' background section of the application. The Examiner's contention that one of ordinary skill in the art would somehow interpret Mathew to disclose sidewall spacers that cause a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers, as recited in claim 1, is entirely without merit, and appears to be completely based on hindsight gleaned from Applicant's specification.

Manocha is directed to an "integrated circuit manufacturing technique that relies on the use of polysilicon fillets for overcoming the well known adverse effects of steep sidewalls produced by anisotropic etching processes and undercuts produced by anisotropic etching of multilayers." (Manocha, Abstract). Manocha does not disclose a FinFET and further appears to

fail to disclose virtually every element recited in claim 1. It is unreasonable to contend, as the Examiner appears to allege, that one of ordinary skill in the art, upon reading Manocha, would suddenly interpret Mathew to disclose the formation of first and second sidewall spacers to cause a topology of a gate to smoothly transition over a fin and first and second sidewall spacers to reduce micromasking effects during etching of the gate, as recited in claim 1.

Additionally, in rejecting independent claim 1 based on Mathew and Lin, the Examiner concedes that Mathew does not disclose sidewall spacers having the width recited in these claims. (Office Action, page 2). The Examiner contends, however, that Lin discloses sidewall spacers having the claimed width and that one of ordinary skill in the art would have found it obvious to combine Mathew and Lin. (Office Action, pages 2 and 3).

Applicants submit that the Examiner has not shown proper motivation to combine Mathew and Lin in the manner suggested. The Examiner relies on Lin for the width of the sidewall spacers recited in claim 1, and states that "[I]t would have been obvious to one skilled in this art to form Mathew's polysilicon sidewall spacers with a width of about 150 Å to about 1000 Å because Lin teaches that polysilicon sidewall spacers are conventionally formed that thick." (Office Action, page 3). Applicants respectfully disagree with the Examiner's conclusion of obviousness. Mathew discloses a vertical double gate semiconductor device in which a silicon fin layer extends vertically from the substrate of the device. Lin discloses a more conventional FET device. (Lin, see Title and Abstract). Applicants submit that these two structures would be recognized by one of ordinary skill in the art as different types of semiconductor FET structures and that specific parameters (such as the width of a spacer) in one device could not simply be applied to the other device. Accordingly, one of ordinary skill in the art reading Lin would not be motivated to use the spacer width disclosed by Lin as the width of the floating gate disclosed

by Mathew. Thus, Applicants submit that the Examiner has not made a *prima facie* case of obviousness with regard to Mathew and Lin.

In previous arguments, the Examiner stated that "Mathew and Lin are both directed to insulated gate field effect transistors (IGFETs) comprising gate sidewall spacers, so one of ordinary skill in the art would have been applied Lin's IGFET gate sidewall spacer width teaching to Mathew's IGFET gate sidewall spacer, particularly insofar as Mathew does not disclose the width of its IGFET gate sidewall spacer." (Final Office Action of September 23, 2005, page 7). In response, Applicants submit that a FET and an IGFET are broad terms in the semiconductor art. There are many different types of IGFETs. Although both Lin and Matthew disclose IGFETs, the IGFETs of Lin and Matthew are significantly different from one another. The device of Mathew, for instance, is a vertical double gate semiconductor device. (Mathew, Abstract). The "vertical" nature of the device of Mathew is clearly illustrated in, for example, Fig. 9, in which the channel in semiconductor layer 18 is vertically raised from substrate 12 and insulator 14. Lin, in contrast, discloses a FET device having a conventional horizontal channel in substrate 12. As can be plainly seen by a comparison of the figures of Lin and Mathew, the two different devices are structurally significantly different from one another. Accordingly, Applicants submit that one of ordinary skill in the art would not be motivated to apply specific parameters (such as the width of a spacer) in one device to the other device. Thus, one of ordinary skill in the art reading Lin would not be motivated to use the spacer width disclosed by Lin as the width of the floating gate disclosed by Mathew

An argument similar to the one given above regarding lack of motivation to combine Mathew and Lin was made by Applicants in the After Final Amendment of November 22, 2005. In response, the Examiner states that "Mathew's and Lin's IGFETs are simply not 'significantly

different from one another' by common IGFET definition, let alone by one skilled in the art familiar with their common gate sidewall spacers feature." (Advisory Action of December 8, 2005, Continuation Sheet). Applicants disagree. Although all IGFETs may be based on the same fundamental operational principles, the design and manufacture of different IGFETs can be significantly different from one another. A simple comparison of the figures (e.g., between Figure 15 of Mathew and Figure 10 of Lin) illustrates the significant differences between construction of a FinFET and a conventional horizontal channel FET. The Examiner can appreciate that these two devices are significantly different structurally and that particular device widths in one device are not likely to be relevant in the other device.

For at least these reasons, Applicants submit that the rejection of claim 1 under 35 U.S.C. § 103(a) based on Mathew and Lin is improper and should be withdrawn. At least by virtue of their dependency on claim 1, the rejections of claims 3, 4, 6, and 7 based on Mathew and Lin are also improper and should be withdrawn.

Claims 16 and 18 additionally stand rejected under 35 U.S.C. § 103(a) based on Mathew and Lin. Applicants respectfully traverse this rejection.

Claim 16 recites, for example, that the first and second sidewall spacers are formed in a "roughly triangular shape" and the gate is formed over the sidewall spacers "whereby the first and second sidewall spacers cause a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers and the first and second sidewall spacers reduce micromasking effects during etching of a gate material to form the gate." As mentioned above, Mathew does not discuss the desirability of causing a topology of the gate to smoothly transition over a fin and the first and second sidewall spacers, and thus, could not possibly disclose or suggest this feature of claim 16. Further, neither Mathew nor Lin in any way disclose or suggest

first and second sidewall spacers that reduce micromasking effects during etching of a gate material to form the gate.

Additionally, in rejecting claim 16, the Examiner relies on Lin for disclosure relating to the claimed width of the sidewall spacers (i.e., as recited in claim 16, that "the first and second sidewall spacers reduce micromasking effects during etching of a gate material to form the gate." For reasons similar to those given above with respect to claim 1, Applicants submit that the Examiner has not made a *prima facie* case of obviousness with regard to Mathew and Lin. That is, Mathew discloses a vertical double gate semiconductor device and Lin discloses a more conventional FET device. These two structures would be recognized by one of ordinary skill in the art as different types of semiconductor FET structures and that specific parameters (such as the width of a spacer) in one device could not simply be applied to the other device. Thus, Applicants submit that the Examiner has not made a *prima facie* case of obviousness with regard to Mathew and Lin.

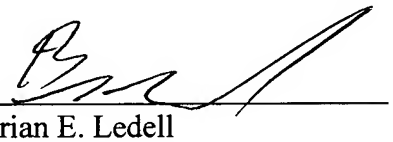
For at least these reasons, Applicants submit that the rejection of claim 16 under 35 U.S.C. § 103(a) based on Mathew and Lin is improper and should be withdrawn. At least by virtue of its dependency on claim 16, the rejection of claim 18 based on Mathew and Lin are also improper and should be withdrawn.

In view of the foregoing amendments and remarks, Applicants submit that the claimed invention is neither anticipated nor rendered obvious in view of the prior art references cited against this application. Applicants therefore request the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY SNYDER, L.L.P.

By: 
Brian E. Ledell
Reg. No. 42,784

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11350 Random Hills Road
Suite 600
Fairfax, Virginia 22030
Telephone: 571-432-0800
Facsimile: 571-432-0808
Customer Number: 45114